PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of

Satoshi SUGAHARA et al.

Application No.: 10/550,652

Filed: September 23, 2005 Docket No.: 125426

For: RECONFIGURABLE LOGIC CIRCUIT USING A TRANSISTOR HAVING SPIN-DEPENDENT TRANSFER CHARACTERISTICS

INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Pursuant to 37 CFR §1.56, the attention of the Patent and Trademark Office is hereby directed to the references listed on the attached PTO-1449. Unless otherwise indicated herein, one copy of each reference is attached. It is respectfully requested that the information be expressly considered during the prosecution of this application, and that the references be made of record therein and appear among the "References Cited" on any patent to issue therefrom.

☒ 1. This Information Disclosure Statement is being filed (a) within three months of the U.S. filing date of this non-CPA application, OR (b) before the mailing date of a first Office Action on the merits in the present application. No certification or fee is required.

☒ 2. Relevance of references 10-15 is discussed in the present specification.

☒ 3. References 1-5 and 7-9 were cited in the International Search Report. An English language version of the International Search Report is attached for the Examiner's information.

☒ 4. English language Abstracts of references 1-5, 7-9, 12 and 15 are attached hereto.

☒ 5. Computer-generated English language translations of the following Japanese references have been obtained from the website of the Japanese Patent Office ([http://www.jpo.go.jp]), and are attached, but have not been reviewed for accuracy. See References 1-5 & 7.

☒ 6. Reference 6 corresponds to Reference 5.

Respectfully submitted,

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JAO:JOC/nxy

Date: October 21, 2005

DEPOSIT ACCOUNT USE AUTHORIZATION
Please grant any extension necessary for entry;
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ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /E.L./

Form PTO-1449 (REV. 8-83) US Dept. of Commerce PATENT & TRADEMARK OFFICE	ATTY DOCKET NO. 125426	APPLICATION NO. 10/550,652
INFORMATION DISCLOSURE STATEMENT (Use several sheets if necessary)	APPLICANTS Satoshi SUGAHARA et al.	
	FILING DATE September 23, 2005	GROUP

U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS
	1.	JP-A-2003-092412 w/ abst. & trans.	03/28/2003	JAPAN		
	2.	JP-A-2003-008105 w/ abst. & trans.	01/10/2003	JAPAN		
	3.	JP-A-11-340542 w/ abst. & trans.	12/10/1999	JAPAN		
	4.	JP-A-2000-349619 w/ abst. & trans.	12/15/2000	JAPAN		
	5.	JP-A-06-250994 w/ abst. & trans.	09/09/1994	JAPAN		
	6.	EP 0 685 808 A1	12/06/1995	EUROPEAN PATENT OFFICE		
	7.	JP-A-05-343984 w/ abst. & trans.	12/24/1983	JAPAN		
	8.	JP-A-61-234623 w/ abst.	10/18/1986	JAPAN		

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)

	9.	S. SUGAHARA et al.; "A Spin MOSFET and its Applications"; The Magnetics Society of Japan; Vol. 134; January 2004; pp. 93-100. (w/ abstract)
	10.	Stephen TRIMBERGER; "A Reprogrammable Gate Array and Applications"; *Proceedings of the IEEE*; Vol. 81, No. 7; July 1993; pp. 1030-1041.
	11.	Scott HAUCK; "The Roles of FPGA's in Reprogrammable Systems"; *Proceedings of the IEEE*; Vol. 86, No. 4; April 1998; pp. 615-638.
	12.	Toshinori SUEYOSHI; "Programmable Logic Devices - from the Past to the Furture"; *Technical Report of IEICE*; Vol. 101, No. 632; 2002; pp. 17-24 (w/ abstract)
	13.	Tadashi SHIBATA et al.; "A Functional MOS Transistor Featuring Gate-Level Weighted Sum and Threshold Operations"; *IEEE Transactions on Electron Devices*; Vol. 39, No. 6, June 1992; pp. 1444-1455.

EXAMINER	/Eugene Lee/	DATE CONSIDERED	10/13/2008

Examiner: Initial if citation considered, whether or not citation is in conformance with M.P.E.P. 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

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OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)

	14.	Tadashi SHIBATA et al.; "Neuron MOS Binary-Logic Integrated Circuits- Part I: Design Fundamentals and Soft-Hardware-Logic Circuit Implementation; *IEEE Transactions on Electron Devices*; Vol. 40, No. 3, March 1993; pp. 570-576.
	15.	Hiroshi SAWADA et al; "Consideration for a Reconfigurable Logic Device using Neuron MOS Transistors"; Technical Report of IEICE; Vol. 99, No. 481; November 1999; pp. 41-48. (w/ abstract)

EXAMINER /Eugene Lee/ DATE CONSIDERED 10/13/2006

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